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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,805	05/28/2004	Jeanne P. Bickford	BUR920040021US1	3804

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EXAMINER	
WALLING, MEAGAN S	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 10/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/709,805	BICKFORD ET AL.
	Examiner	Art Unit
	Meagan S. Walling	2863

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-15* is/are allowed.

6)☒ Claim(s) *1,3,4,6,8 and 9* is/are rejected.

7)☒ Claim(s) *2,5,7 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: _____.

DETAILED ACTION

Specification

The abstract of the disclosure is objected to because it exceeds 150 words.

Correction is required. See MPEP § 608.01(b).

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1, 3, 4, 6, 8, and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsumoto et al. (US 2005/0017746).

Regarding claim 1, Matsumoto et al. teaches measuring resistances on a plurality if manufacturing test structures within a wafer running on a wafer manufacturing line (par. 47); obtaining an actual distribution value based on the result of the measured resistances on the plurality of manufacturing test structures (par. 47); measuring resistances on a plurality of design test structures within the wafer (par. 47); correlating the measured resistance of the design test structures to the measured resistance of the manufacturing test structures to obtain an offset value

(par. 47); and adjusting resistances of an adjustable resistor circuit within the wafer and subsequent wafers running on the wafer manufacturing line according to the offset value (par. 48).

Regarding claim 3, Matsumoto et al. teaches monitoring manufacturing test structures on wafers of the wafer manufacturing line (par. 2).

Regarding claim 4, Matsumoto et al. teaches adjusting resistances of an adjustable resistor circuit within a wafer on the manufacturing line according to the offset value if the resistance of the manufacturing test structure on the wafer falls within a target resistance range (par. 28).

Regarding claim 6, Matsumoto et al. teaches a means for measuring resistances on a plurality if manufacturing test structures within a wafer running on a wafer manufacturing line (par. 47); means for obtaining an actual distribution value based on the result of the measured resistances on the plurality of manufacturing test structures (par. 47); means for measuring resistances on a plurality of design test structures within the wafer (par. 47); means for correlating the measured resistance of the design test structures to the measured resistance of the manufacturing test structures to obtain an offset value (par. 47); and means for adjusting resistances of an adjustable resistor circuit within the wafer and subsequent wafers running on the wafer manufacturing line according to the offset value (par. 48).

Regarding claim 8, Matsumoto et al. teaches means for monitoring manufacturing test structures on wafers of the wafer manufacturing line (par. 2).

Regarding claim 9, Matsumoto et al. teaches means for adjusting resistances of an adjustable resistor circuit within a wafer on the manufacturing line according to the offset value

if the resistance of the manufacturing test structure on the wafer falls within a target resistance range (par. 28).

Allowable Subject Matter

2. Claims 2, 5, 7, and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The primary reason for the indication of allowability of claims 2 and 7 is the inclusion of the limitation of recording and means for recording the difference between the actual distribution value and a predetermined distribution value, wherein the predetermined distribution value is obtained based on a ground rule resistance. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art of record that makes these claims allowable.

The primary reason for the indication of allowability of claims 5 and 10 is the inclusion of the limitation of discarding and means for discarding a wafer if the resistance of the manufacturing test structures on the wafer does not fall within the target resistance range. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art of record that makes these claims allowable.

3. Claims 11-15 are allowed.

The following is an examiner's statement of reasons for allowance:

The primary reason for the allowance of claim 11 is the inclusion of the limitation of program code means for measuring resistances on a plurality if manufacturing test structures within a wafer running on a wafer manufacturing line; program code means for obtaining an actual distribution value based on the result of the measured resistances on the plurality of manufacturing test structures; program code means for measuring resistances on a plurality of design test structures within the wafer; program code means for correlating the measured resistance of the design test structures to the measured resistance of the manufacturing test structures to obtain an offset value; and program code means for adjusting resistances of an adjustable resistor circuit within the wafer and subsequent wafers running on the wafer manufacturing line according to the offset value. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art of record that makes these claims allowable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Meagan S. Walling whose telephone number is (571) 272-2283. The examiner can normally be reached on Monday through Friday 8:30 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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BRYAN BUI
PRIMARY EXAMI